UNIVERSITY OF BUDAPEST

J750EX\textsuperscript{HD} INTRODUCTION

5. July 2016
Guenther Liebl, Manfred Graf
AGENDA

- Welcome
- The J750 Tester Platform
  - Market Position
  - J750EX^{HD} Architecture
  - J750EX^{HD} Instrumentation
  - IG-XL Tester Software
- Local Support
- Wrap Up
Teradyne 750 Platform:

- WW Leader for Microcontroller Test
- WW Leader for Image Sensor Test
- Extending capabilities for Digital Wafer Sort
- J750EX\textsuperscript{HD} roadmap enables 2X site count
- >5000\textsuperscript{th} System shipped in Q3 2015, Biggest ATE Installed Base
INSTALLED BASE: CURRENT GENERATION TESTERS

North America:
- **1,715 Systems**
  - FLEX: 256 Systems
  - UltraFLEX: 228 Systems
  - J750: 356 Systems
  - ETS: 581 Systems
  - Magnum: 294 Systems

Europe:
- **978 Systems**
  - FLEX: 274 Systems
  - UltraFLEX: 39 Systems
  - J750: 411 Systems
  - ETS: 145 Systems
  - Magnum: 109 Systems

China:
- **1,600 Systems**
  - FLEX: 175 Systems
  - UltraFLEX: 102 Systems
  - J750: 665 Systems
  - ETS: 483 Systems
  - Magnum: 175 Systems

Korea:
- **1,295 Systems**
  - FLEX: 120 Systems
  - UltraFLEX: 268 Systems
  - J750: 380 Systems
  - ETS: 141 Systems
  - Magnum: 386 Systems

Japan:
- **1,444 Systems**
  - FLEX: 99 Systems
  - UltraFLEX: 60 Systems
  - J750: 1,296 Systems
  - ETS: 51 Systems
  - Magnum: 38 Systems

S.E. Asia:
- **4,426 Systems**
  - FLEX: 908 Systems
  - UltraFLEX: 335 Systems
  - J750: 1,275 Systems
  - ETS: 1,447 Systems
  - Magnum: 449 Systems

Taiwan:
- **2,430 Systems**
  - FLEX: 435 Systems
  - UltraFLEX: 484 Systems
  - J750: 1,098 Systems
  - ETS: 193 Systems
  - Magnum: 220 Systems

80% of systems are installed in Asia
J750EX-HD Wins EDN's 2014 Best in Test Award for Manufacturing Test
January 30, 2014
AGENDA

- Welcome
- The J750 Tester Platform
  - Market Position
  - J750EX\(^{HD}\) Architecture
  - J750EX\(^{HD}\) Instrumentation
  - IG-XL Tester Software
- Local Support
- Wrap Up
The 750 Platform

J750

J750Ex

J750ExHD
J750 & IP750 PRODUCT LINE
MARKET EXPANSION FOR THE J750 PLATFORM

High Speed Digital Instruments
- **HSD100**
  - 1998 to 2014 – 16 yrs
  - 64 ch 100MHz
- **HSD200 (2007)**
  - 64 ch 200MHz

Performance DC Instruments
- **DPS**
  - 8 ch 10V 1A
- **APMU**
  - 64 ch 35V 50mA
- **CTO**
  - 8 ch src/cap/Ref 16 bit

Performance Analog Instruments
- **MSO**
  - 4ch AWG; 4ch DIG
- **RFID**
  - 16 ch src and capture

Imager Sensor Test Products
- **IP750EX**
  - **ICMD** (MIPI 1.5G)
  - **ICUL1G** (LVDS 1G)
  - **ICUA2**
  - **ICUD200**

HD Instrument Family
- **HSD800 (2014)**
  - 128 ch 400MHz
- **HD VIS**
  - 24 ch ±10V ±200mA
- **HD DPS**
  - 24 ch/48 ch, 11V 1A
- **HD CTO**
  - 32 src, 8 cap, 32 Vref
  - 17-bit INL
  - 100kHz AC source
- **HD APMU** (Dec 2013)

Teradyne J750Ex HD architecture and instruments:
- Lowering Cost of Test while maintaining compatibility
- Reduce single site test time,
- Increase parallel test efficiency
J750 HARDWARE TECHNICAL OVERVIEW

J750 System Types and Configurations

- J750 (with HSD100), J750EX (with HSD200) and J750EX^{\text{HD}} (with HSD800)
- Two sizes: 8 digital slots or 16 digital slots
**J750EX**

- **HSD800 or HDDPS**
  - Multi-Function Digital
  - DPS Instrument

- **HDDPS or HDVIS**
  - V/I Instrument

- **HDCTO**
  - Analog Option

- **Power Switch & Kinematic Coupler-Controller Connector**

- **Fan Assembly**

- **Power Supply Assemblies**

**Center - 9 Half-Width Cards:**
4 HDDPS/HDVIS, 4 HDCTO, 1 CALCUB

**Sides – 8/16 Full-Width Cards:**
8 digital cards (up to 1024 channels) or 16 digital cards (up to 2048 channels)

©2016 Teradyne Inc. - All Rights Reserved - Teradyne Confidential
System Broadcast Feature: Distributed Local Controllers

- During test program **validation** the host controller loads test information to the local controllers.
- During **run time** the host controller executes a high level command and the local controllers setup all channels in parallel.

**Time Sets (Basic)**

<table>
<thead>
<tr>
<th>Time Set</th>
<th>Cycles</th>
<th>Test Group</th>
<th>Data</th>
<th>Shift 1</th>
<th>Shift 2</th>
<th>Shift 3</th>
<th>Shift 4</th>
<th>Shift 5</th>
<th>Shift 6</th>
<th>Shift 7</th>
<th>Shift 8</th>
<th>Mode</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td>fntx_e0</td>
<td>20, E-09</td>
<td>t test</td>
<td>PAT</td>
<td>6.9E-09</td>
<td>9.9E-09</td>
<td>19.9E-09</td>
<td>0 Off</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fntx_e0</td>
<td>20, E-09</td>
<td>l std</td>
<td>PAT</td>
<td>1.4E-09</td>
<td>4.4E-09</td>
<td>0.4E-12</td>
<td>Edge</td>
<td>6.9E-09</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fntx_e0</td>
<td>20, E-09</td>
<td>l std</td>
<td>PAT</td>
<td>9.7E-09</td>
<td>12.7E-09</td>
<td>0.1E-12</td>
<td>Edge</td>
<td>6.9E-09</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fntx_e0</td>
<td>20, E-09</td>
<td>l std</td>
<td>PAT</td>
<td>1.4E-09</td>
<td>4.4E-09</td>
<td>0.4E-12</td>
<td>0 Off</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>fntx_e0</td>
<td>20, E-09</td>
<td>l std</td>
<td>PAT</td>
<td>9.7E-09</td>
<td>12.7E-09</td>
<td>0.1E-12</td>
<td>Edge</td>
<td>6.9E-09</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

- Time Set Download
- Level Set Download
- Connections (PE, PPMU, BPMU, DIB Access)
- Hardware Calibration Factors
- Hardware Averaging
- Hardware Limits
**J750EX<sup>HD</sup> INTRODUCTION / OVERVIEW**

### Hardware:
- **HSD800**
  - Digital card
- **HDCTO**
  - Analog option
- **HDVIS**
  - V/I Instrument
- **HDDPS24/48**
  - DPS Instrument

### Software:
- **IG-XL Software**
  - Win7 / Office 2010
- **Tera1**
  - Workstation

### Feature Table:

<table>
<thead>
<tr>
<th>Feature</th>
<th>Throughput Benefit</th>
<th>TTP Benefit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Optimal performance/high density instruments</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Multi-function instrument pins</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>System Broadcast</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>IG-XL Software</td>
<td></td>
<td>X</td>
</tr>
<tr>
<td>Concurrent Test</td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>Upgradeable &amp; Compatible to the ATE industry’s Largest IB</td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>
AGENDA

- Welcome
- The J750 Tester Platform
  - Market Position
  - J750EXHD Architecture
  - J750EXHD Instrumentation
  - IG-XL Tester Software
- Local Support
- Wrap Up
## NEW J750EX PLATFORM INSTRUMENTATION

<table>
<thead>
<tr>
<th>HSD800</th>
<th>HDCTO</th>
<th>HDVIS</th>
<th>HDDPS</th>
<th>J750RF</th>
</tr>
</thead>
<tbody>
<tr>
<td>✓ Multifunction</td>
<td>✓ Analog option</td>
<td>✓ V/I Instrument</td>
<td>✓ DPS Instrument</td>
<td>✓ RF Instrument</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Digital</th>
<th>Precision AC/DC Src/Cap/Volt Ref</th>
<th>Precision V/I</th>
<th>HD DPS</th>
<th>J750RF Option</th>
</tr>
</thead>
<tbody>
<tr>
<td>Key MCU Requirements</td>
<td>Higher Site counts. Higher Speed, multi-function device pins</td>
<td>Test Coverage for embedded SAR and Sigma Delta Converters. Increased Numbers of ADC and AC/DC Performance per device</td>
<td>Low current measurements for MCU Sleep Mode</td>
<td>Higher Number of Device Power Supplies for Higher Site Counts</td>
</tr>
<tr>
<td>J750 Feature</td>
<td>800Mbps 12 18V Pins GbE Datalink AutoStrobe DSSC w/VSS DIB Access DS HRAM 8K SVM</td>
<td>32-ch Source 17-bit INL for SAR ADC 100kHz for ΣΔ (100dB THD @ 1KHz) 8-ch Capture 100kHz Capture 15-bit INL 32-ch Vref Up to ±60µV accuracy</td>
<td>24-channels +/-25nA Measure Acc 200mA/11V Merge to 800mA ADC/ch</td>
<td>24 or 48-channels 1A, -2V to 11V Merge to 24A ADC/Ch Slew rate control</td>
</tr>
</tbody>
</table>
J750EX<sup>HD</sup> Instruments

- **HSD800 multi-function digital channel card**
  - 128 digital channels with PPMU
  - 800Mbps
  - 128M Vector Memory, Scan Option, Memory Test Option, DSSC
  - 12 High Voltage Channels: 18V / 100mA
  - 32 Fast High Voltage Channels: 13V / 12mA

- **HDDPS**
  - 24 or 48 digital power supplies per card
  - -2V /11V, 1A single channel, 24A merged

- **HDVIS**
  - 24 V/I resources: +/-10V / 200mA

- **HDCTO**
  - 32 AWG, 32 V-Reference and 8 Digitizer per Half Slot Instrument Card (max 4)
  - High linearity ramp generator for 14-bit ADC testing
  - Sine wave and AWG modes for AC testing of SAR and Delta-Sigma ADCs
  - Bandwidth 100kHz, sample rate 0 to 250kHz, 64k/128k sample memory

- **Other Instrument Options**
  - DC: APMU, DPS, HVDPS
  - AC: MSO
  - RF: LitePoint
Up to 512 sites supported natively in IG-XL → Aligned to digital, MCU multi-function and reduced pin count test strategies

Each HSD800 digital channel board includes the following features

- 128 multi functional channels
- Up to 400MHz clocks and **800Mbps for drive and receive** in multiplex mode
- Drive levels: -1.5V to +6.5V, with 1mV resolution
- **12 high-voltage drive pins**, 0V to +18V DC, 12 channels at 100mA each
- **32 fast slew rate high-voltage drive pins**, 0V to +13V, 32 channels at 12mA each
- Comparator threshold range: -1.5V to +6.5V with <1mV resolution
- Large Vector Memory (LVM): 128M with maximum license
- Additional per pin resources: PPMU, Active Load Circuit, Dynamic Voltage Clamps, Frequency Counter
- **Two ±24V, 200mA four quadrant, force and measure BPMUs**
- Gigabit Ethernet pattern loading and captured data readback
- Eight DIB access pins per 128 channels (two per 32 channels)
- AutoStrobe for single pattern device edge search
- DVM, Frequency Counter
- Optional DSIO source/capture engines (six on each group of 64 channels), **Virtual Sites**
- Optional SCAN feature with up to 3G scan chain depth
- Optional 16M x 96 bit Deep Scan HRAM (DSHRAM) for capture of Scan vector data
- Optional MTO with algorithmic address and data generation for testing embedded memories
System Broadcast Feature: **SiteSmart Pins**

Tester channels are site and pin aware

One broadcast command sets up multiple pins and multiple sites in parallel

Tester channel is site and pin aware

TheHdw.PPMU.Pins("PinA, PinB").Force(5V)
J750EX-HD HIGH-SPEED DATA LINK

Fast Pattern Load

- 280 I/O 32-Bit MCU Program with ~12M LVM
- 14 min to 3 min (5x Improvements)
- Reduce change over time and improve OEE

Independent High-speed GBIT Data Link Per Board for DSSC/MTO/DSHRAM
**AUTO STROBE – FAST EDGE SEARCHES**

### Traditional Edge Search Methodology

- **Program Initial Strobe Timing**
  - Pattern Burst
  - Read Pass/Fail

- **Modify Strobe Timing**
  - Pattern Burst
  - Read Pass/Fail

- **Program Strobe Timing**
  - Pattern Burst
  - Read Pass/Fail

### AutoStrobe Use Model

- **Program AutoStrobe Timing**
  - Pattern Burst
  - Read Edge Location

**SETUP + ONE PATTERN BURST + READ RESULT!**

**HOST PC & PATTERN BURST PER POINT**

**Single Site Test Time:**
- **Edge Search:** 11.5ms
- **AutoStrobe:** 2.1ms

Note: The Edge Search and Auto Strobe tests used the same pattern and assumed 10ns search window with 100ps resolution.
AUTO STROBE PROGRAMMING MODEL

• Use for edge searches and DUT timing characterization
  - Measure pulse width, duty cycle or clock jitter in a single pattern burst

Auto Strobe User Programmable Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Label + Offset</td>
<td>Determines start vector for the first strobe</td>
</tr>
<tr>
<td>StartTime</td>
<td>Time within the start vector for the first strobe</td>
</tr>
<tr>
<td>Cycles per Sample</td>
<td>Frequency of Strobe in number of tester cycles</td>
</tr>
<tr>
<td>Step Time</td>
<td>Strobe step increment (minimum = 4ps)</td>
</tr>
<tr>
<td>Samples per Step</td>
<td>Number of samples to take at each time step</td>
</tr>
<tr>
<td>Number of Samples</td>
<td>Total number of strobes (4096 max)</td>
</tr>
</tbody>
</table>

Interpreting the parameters for this example:

• Each green vertical line represents a sample.
• A total of 9 samples are taken with 3 samples per step, which means 3 steps are performed.
• The samples begin 4 vectors after the vector with label “StartVec” at T0 + 10ns.
• The Step increment is 20ns, 3 samples will be taken at 10ns, 3 at 30ns, and 3 at 50ns.
• A sample is taken every other (2nd) cycle

Captured Data = 0 0 0 0 0 0 1 1 1
**EXTERNAL DVM CONNECTION**

**Agilent 3458A External Meter**

May be connected to any BPMU, HV, FHV, PPMU, Digital Pin, or DIB Access Pin

DUT is connected when the PPMU or a Digital Pin is connected.
DVM Access to the Digital Channel Relay Matrix

- Connect High Side of the Meter to (low side automatically goes to DGS):
  - BPMU Force/Sense
  - Connect to any channel’s PPMU
  - Connect to any Channel’s Driver/Comparator/Load and DUT pin
  - Connect to any High Voltage or Fast High Voltage pin
  - Connect to any DIB Access Pin

Advantages and Use Cases:

- Spot calibrate BPMU or PPMU for more accurate voltage forcing and measuring of precision DC signals such as band-gap references
- Source Instrument spot calibration:
  - During a calibration test, apply source voltage, then measure source with meter
  - During DUT test, apply delta offset to programmed voltage.
- Measure Instrument spot calibration:
  - During a calibration test, measure DUT voltage (or a DUT proxy such as PPMU or BPMU) with both the measure instrument and the meter.
  - During DUT test, apply delta offset to the result taken by measure instrument.
HDCTO FEATURES

- 32 Source, 32 Voltage Reference, and 8 Capture per Half Slot Instrument Card (max 4)
- High linearity ramp generator for 14-bit ADC testing
- Sine wave and AWG modes for AC testing of SAR and Sigma-Delta ADCs
- Precision DC capture for 12-bit DAC testing
- Single-ended and differential modes of operation
- Default mode of operation is CTO compatible mode (test program & DIB compatible)
## HDCTO CONVERTER TEST OPTION

<table>
<thead>
<tr>
<th>Feature</th>
<th>HD CTO</th>
</tr>
</thead>
<tbody>
<tr>
<td># “Slices” / Instrument</td>
<td>8</td>
</tr>
<tr>
<td># Sources</td>
<td>4 sources per slice (1 unique x4 fan-out)</td>
</tr>
<tr>
<td># Captures</td>
<td>1 capture per slice</td>
</tr>
<tr>
<td># Voltage References</td>
<td>4 VREF per slice (1 unique x 4 fan-out)</td>
</tr>
<tr>
<td>Max channels per systems</td>
<td>128 source, 32 capture, 128 references</td>
</tr>
<tr>
<td><strong>ADC Test Features</strong></td>
<td></td>
</tr>
<tr>
<td>DSSC</td>
<td>Supported in HDCTO Templates</td>
</tr>
<tr>
<td>Smooth Ramp Mode</td>
<td>Yes - <em>Device limited acquisition time</em></td>
</tr>
<tr>
<td>Superior DC Linearity</td>
<td>17-bit INL (+/- 6ppm)</td>
</tr>
<tr>
<td>Sine Wave Mode</td>
<td>Yes - <em>AC Testing Capability</em></td>
</tr>
<tr>
<td>AWG Sample Rate</td>
<td>250 ksps</td>
</tr>
<tr>
<td><strong>DAC Test Features</strong></td>
<td></td>
</tr>
<tr>
<td>Capture Sample Rate</td>
<td>250 ksps</td>
</tr>
<tr>
<td>Capture Depth</td>
<td>128k</td>
</tr>
<tr>
<td>PPMU</td>
<td>Yes</td>
</tr>
</tbody>
</table>
- HDCTO source is faster than CTO for > 66ksps ADC

- Example Data Acquisition:
  12-bit, 1Mmps ADC, 10 hits per code
  CTO: 614ms
  HDCTO: 41ms
HDDPS FEATURE OVERVIEW

- 24 channels half slot, 48 channels full slot
- -2V to +11V, up to 1A,
- Merge channels to support up to 24A
- Fast load regulation < 20us
  less than 75mV with 800mA step, 10uF
- ADC per-channel, measure current or voltage
  - Five current measurement ranges, 50µA to 1A,
    and two voltage ranges, 4V and 1
  - 16-bit ADC
  - 1K measurement memory
  - 8K waveform capture memory
  - Programmable measure rate, 5µs to 5ms
  - Trigger modes TCIO or External (pattern synchronized)
- Spike Check Tool
  - Leveraged from UltraVI80
- External Source and Capture trigger capability
24 Channels per Card
- Voltage Range from -10V to 10V
- 200mA (normal mode) to 800mA (merged 4 mode)
- Four Quadrant operation
- FV/MI: Force Voltage/Current Measure Mode
- FI/MV: Force Current/Voltage Measure Mode
- MV: Voltage Measure Mode (with High Impedance Output)
- Fast Parallel Measurement per channel ADC
- External Trigger for Digitizer (Capture) and AWG (Source)
- 5µs to 5ms in 5µs steps,
- 8k Samples Capture and 1k Samples Source per Channel
- Trigger Source DAC by External Send input
- Ramp Mode: 64k max. Ramp Size
- Hardware Averaging
- All setups can be stored in Setup Memory
- Setup Memory Size: 2K
### J750 PERFORMANCE OVERVIEW & COMPARISON

<table>
<thead>
<tr>
<th>Parameter</th>
<th>DPS</th>
<th>HDDPS</th>
<th>HDVVIS</th>
<th>HDAPMU</th>
</tr>
</thead>
<tbody>
<tr>
<td>Voltage Range</td>
<td>0 to 10V</td>
<td>-2V to 11V</td>
<td>-10V to 10V</td>
<td>-35V to 35V</td>
</tr>
<tr>
<td>Max Channel Count</td>
<td>32</td>
<td>&gt;336</td>
<td>96</td>
<td>256</td>
</tr>
<tr>
<td>Current Capabilities</td>
<td>1A @ 10V</td>
<td>1A @ 10V (DPS)</td>
<td>200mA @ 10V</td>
<td>50mA @ 35V</td>
</tr>
<tr>
<td></td>
<td>Merge x8 / 8A</td>
<td>Merge x24 / 24A</td>
<td>Merge x4 / 800mA</td>
<td>Merge x8 / 400mA</td>
</tr>
<tr>
<td>Force Voltage Accuracy</td>
<td>±(0.1% + 10mV)</td>
<td>±(0.1% + 4mV)</td>
<td>±(0.1% + 5mV)</td>
<td>5V: ±(0.1% + 2mV)</td>
</tr>
<tr>
<td>Current Accuracy</td>
<td>L: ±(0.1% + 6mA)</td>
<td>L: ±(0.5% + 3mA)</td>
<td>F: ±(0.2% + 0.2mA)</td>
<td>F: ±(0.2% + 50uA)</td>
</tr>
<tr>
<td>Droop/Kick</td>
<td>±250mV typical</td>
<td>±75mV (800mA step)</td>
<td>±450mV (100mA step)</td>
<td>±100mV (5mA step)</td>
</tr>
</tbody>
</table>

### Current Measure Accuracy

<table>
<thead>
<tr>
<th>Current Measure Accuracy</th>
<th>DPS</th>
<th>HDDPS</th>
<th>HDVVIS</th>
<th>HDAPMU</th>
</tr>
</thead>
<tbody>
<tr>
<td>200nA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>2uA</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>5uA/10uA</td>
<td></td>
<td></td>
<td>5uA: ±20nA</td>
<td>5uA: ±(0.2% + 25nA)</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>10uA: ±(0.2% + 50nA)</td>
<td></td>
</tr>
<tr>
<td>50uA</td>
<td></td>
<td></td>
<td>±(0.1% + 100nA)</td>
<td>±(0.2% + 125nA)</td>
</tr>
<tr>
<td>500uA</td>
<td></td>
<td></td>
<td>±(0.1% + 0.5uA)</td>
<td>±(0.2% + 0.5uA)</td>
</tr>
<tr>
<td>5/10mA</td>
<td>10mA: ±(0.1% + 25uA)</td>
<td>10mA: ±(0.1% + 10uA)</td>
<td>5mA: ±(0.2% + 5uA)</td>
<td>5mA: ±(0.2% + 5uA)</td>
</tr>
<tr>
<td>50/100mA</td>
<td>0.1A: ±(0.1% + 250uA)</td>
<td>0.1A: ±(0.1% + 100uA)</td>
<td>50mA: ±(0.2% + 50uA)</td>
<td>50mA: ±(0.2% + 50uA)</td>
</tr>
<tr>
<td>200mA</td>
<td></td>
<td></td>
<td>±(0.1% + 2mA)</td>
<td></td>
</tr>
<tr>
<td>1A</td>
<td></td>
<td></td>
<td>±(0.2% + 200uA)</td>
<td></td>
</tr>
</tbody>
</table>
J750-LITEPOINT RF TEST SOLUTION

DC, AC, Digital

BASEBAND

RF

DSP Built-In

LitePoint Control

J750 Control

System link

Ethernet control

Event Trigger / Flag

10MHz clock Ref

software

IG·XL

©2016 Teradyne Inc. - All Rights Reserved - Teradyne Confidential
RF Upgrade to J750
✓ Available as an upgrade for all J750 models (J750, Ex, HD)
✓ Compatible with existing J750 instruments and hardware options

Complete integration to J750 HW & SW
✓ Leverage IG-XL for development & debug
✓ Incorporates LitePoint RF Tool Suite and modulation libraries

Optimized RF Signal Delivery Design
✓ Support for up to 32 RF ports enables high site counts
✓ Reliable signal interface for 6GHz performance to DIB

Configurable LitePoint Options
✓ Scalable configurations for Cellular & Connectivity RF applications
✓ Local DSP in each LitePoint system for fast background calculations
✓ Compatible with existing LitePoint applications

Key Features

Integrated RF signal delivery
Common development and debug control

Configurable LitePoint instrumentation
J750-LITEPOINT RF OPTIONS

IQxel-M6

Connectivity

- WiFi
- MIMO
- Bluetooth 1 - 4.0 (LE)
- 4G WiMAX
- Zigbee
- FM
- GPS / GLONASS

IQxel-M8

Connectivity

- WiFi
- MIMO
- Bluetooth 1 - 4.0 (LE)
- 4G WiMAX
- Zigbee

IQxstream

Cellular

- WiFi (2.4G band)
- Bluetooth
- GSM / EDGE
- W-CDMA
- CDMA2000 / EV-DO
- TD-SCDMA

©2016 Teradyne Inc. - All Rights Reserved - Teradyne Confidential
AGENDA

- Welcome
- The J750 Tester Platform
  - Market Position
  - J750EXHD Architecture
  - J750EXHD Instrumentation
  - IG-XL Tester Software
- Local Support
- Wrap Up
Teradyne has been ranked #1 in ATE Software for the last three years by VLSI Customer Satisfaction Research Research Survey, **CMMI level 3**

30% faster test program development time

- Native MultiSite, Program Modularity, Templates, “Debug in the Zone”, Complete tool set

Optimal throughput early in the product ramp resulting in faster time to profits.

- IG-XL’s Pure Parallel, Native Multi Site, System Broadcast,

Faster time to entitled yield

- Scan fail capture throughput, APIs to design environments

Better quality programs that result in fewer RMAs and defect escapes

- VBT, Simulation Tools, Version Control

New users become self sufficient faster

- Easy to learn programming language, DUT Centric use model, Template programming
WHAT IS IG-XL?

- Device Centric Programming
- Common programming model between instrument families
- Easy to learn. Context sensitive help and auto complete
- Removes opportunity for costly coding mistakes
- Automatic management of threading and background execution for DSP and Concurrent Test

Excel

- Familiar tool to all engineers
- Easy data entry with formula support
- Separation of Data and Method for easy code re-use
- Easy to extend & customize

VBT

- Complete set of tools that span the entire semi space
- Integrated Analog and Digital tools
- Modular and Collaborative development

IG-XL Tools

©2016 Teradyne Inc. - All Rights Reserved - Teradyne Confidential
VBT: THE RIGHT LANGUAGE FOR ATE

EASY
- Based on VBA
- Easy to use IDE with Intellisense™
- Consistent use model across instruments
- Easy to extend – Many user generated plug ins available on eKnowledge

POWERFUL
- Less than 50% lines of code compared to other ATE programming languages
- Easy to create reusable code libraries
- Object Oriented
- “Debug In The Zone” – No compilation required!
- Native Multisite

SAFE
- No chances for memory leaks
- Threading complexity is handled by ATE not user
IG-XL HAS A NATIVE MULTI-SITE ARCHITECTURE

IG-XL’s native multi-site test development environment eliminates the ‘multi-site’ tax in conventional ATE software

- Automatic management of multi-site data
- User writes a single-site test program and it automatically scales
- IG-XL manages site awareness, scaling, exception handling aspects of single site work
- Introduction of PinListData and Site Variables with IG-XL 3.50.40

IG-XL delivers the fastest time to completion for multisite programs

TER Multisite conversion step

Conventional Software

IG-XL

Total Program Development Time (Hours)

©2016 Teradyne Inc. - All Rights Reserved - Teradyne Confidential
Easy to use Flow Sheet based use model, IG-XL v3.60

Flow Table

<table>
<thead>
<tr>
<th>Command</th>
<th>Opcode</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test</td>
<td></td>
<td>Continuity</td>
</tr>
<tr>
<td>Test</td>
<td></td>
<td>Flash</td>
</tr>
<tr>
<td>Test</td>
<td></td>
<td>ADC</td>
</tr>
<tr>
<td>Test</td>
<td></td>
<td>Scan</td>
</tr>
<tr>
<td>Test</td>
<td></td>
<td>Func_PLL</td>
</tr>
<tr>
<td>Test</td>
<td></td>
<td>Func_Mon</td>
</tr>
<tr>
<td>Test</td>
<td></td>
<td>Func_WDT</td>
</tr>
</tbody>
</table>

Flow Table

<table>
<thead>
<tr>
<th>Command</th>
<th>Opcode</th>
<th>Parameter</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test</td>
<td>Test_StartBP</td>
<td>Flash</td>
</tr>
<tr>
<td>Test</td>
<td>Test_EndBP</td>
<td>ADC</td>
</tr>
<tr>
<td>Test</td>
<td>Test_StartBP</td>
<td>Scan</td>
</tr>
<tr>
<td>Test</td>
<td>Test_EndBP</td>
<td>Func_Mon</td>
</tr>
<tr>
<td>Test</td>
<td>Test</td>
<td>Func_PLL</td>
</tr>
<tr>
<td>Test</td>
<td>Test</td>
<td>Func_WDT</td>
</tr>
</tbody>
</table>

Foreground Pattern Domain

Background Pattern Domain

Fast, Simple Changes

SIGNIFICANT THROUGHPUT BENEFIT
AGENDA

- Welcome
- The J750 Tester Platform
  - Market Position
  - J750EXHD Architecture
  - J750EXHD Instrumentation
  - IG-XL Tester Software
- Local Support
- Wrap Up
Local J750 Teradyne Experts available

- Munich:
  - 10+, 100+ man years MCU experience
  - J750 product specialist
- Other Europe: 10+
- Global Support Structure for Apps Support

- Training Rooms in Munich
- J750 and J750EX<sup>HD</sup> tester in Munich
- PCB Design Team in Munich
J750EX<sup>HD</sup> – Fastest Time to Profit

J750 is Available Everywhere
Leveraging >5,000 Installed Base Ecosystem Worldwide

- Ability to reuse existing J750 and J750EX installed base
- Test Floor Space and Peripherals Savings – Cost Avoidance
- Lowest Transition Cost (no employee cross training, no retooling)

Reduce the Cost of Test 25% to 50% with Higher Throughput

- Higher site count delivered by HD Family of Instruments
- New Single-site and Multi-site Throughput Features (Example: Gigabit Ethernet, Concurrent Test)

Fastest Time for Production

- IG-XL Multi Site Program Development Capability
- Lowest Risk in Production bring up by leveraging current docking and production floor processes
YOUR REQUIREMENTS
YOUR TESTER REQUIREMENTS

- Wafer/Final Test
- Digital Pin Count, Speed, Memory Depth
- Power Supply Pin Count, max. Voltage and Current
- VI Pin Count, max. Voltage and Current
- ADC/DAC, INL/DNL, THD, SNR
- Digital Options (LVM, Speed, SCAN, DSSC, …)
THANK YOU